AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.(Currently Amended) A communication unit for a multiple code rate communication system comprising:

a codeword defining N codeword elements and K information elements coded at a code rate R=K/(N-P), wherein P is a number of punctured elements of the codeword;

a first storage location for storing an error reduction code mother code definition;

a second storage location for storing a maximum puncture sequence S_{max}, wherein the maximum puncture sequence S_{max} is stored in and retrieved from a plurality of memory elements, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a minimum puncture sequence ~~subset~~ S_1 that is a puncture sequence for a minimum code rate R_1, wherein the minimum puncture sequence S_1 is stored in and retrieved from a subset of the plurality of memory elements that store the maximum puncture sequence S_{max}, wherein the codeword is one of decoded or encoded through the error reduction code mother code definition read from the first storage location and a selected one of puncturing sequences S_1, S_2, ...S_{max} read from the second storage location, wherein the sequence S_2 is stored in and retrieved from a subset of the plurality of memory elements that store the maximum puncture sequence S_{max}.

2.(Previously Presented) The communication unit of claim 1 wherein the unit is one of a transmitter that outputs the codeword or a receiver that receives the codeword.

3.(Previously Presented) The communication unit of claim 1 wherein $S_{max}=S_{N-K}$.

4.(Currently Amended) The communication unit of claim 1 wherein the maximum puncture sequence S_{max} further comprises at least two sequences ~~subsets~~ S_i that are puncture sequences for code rates R_i, wherein *i* is an integer greater than or equal to one and each sequentially higher i^{th} code rate is higher than the sequentially lower i^{th} code rate, wherein each of the sequences S_i is stored in a unique subset of the plurality of memory elements that store the maximum puncture sequence S_{max}.

5.(Currently Amended) The communication unit of claim 4 wherein each sequence S_i is stored in ~~comprises~~ at least one memory element, and each sequence S_i with at least two memory elements has at least one memory element in common with another sequence S_i and with the maximum puncture sequence S_{max}, wherein each of the sequences S_i is stored in a unique subset of the plurality of memory elements that store the maximum puncture sequence S_{max}.

6.(Original) The communication unit of claim 4 wherein $S_1 \subseteq S_2 \subseteq \ldots \subseteq S_{max-1} \subseteq S_{max}$.

7.(Currently Amended) The communication unit of claim 1 wherein the second storage location comprises a plurality of memory elements for storing the maximum puncture sequence S_{max}, each memory element storing a variable degree.

8.(Currently Amended) The communication unit of claim 1 wherein the second storage location comprises a plurality of memory elements for storing the maximum puncture sequence S_{max}, each memory element storing a variable node location.

9.(Currently Amended) The communication unit of claim 1 wherein the second storage location comprises a plurality of memory elements for storing the maximum puncture sequence S_{max}, each memory element storing one of a variable degree, a check degree, a variable node location, or a check node location.

10.(Original) The communication unit of claim 1 wherein the error reduction code mother code is a low-density parity-check (LDPC) mother code.

11.(Previously Presented) A transceiver for transmitting and receiving a codeword at any of three coding rates R_1, R_2 and R_3, wherein the codeword defines N codeword elements, K information elements, and P punctured elements, and the coding rates $R_1=K/(N-P_1) < R_2=K/(N-P_2) < R_3=K/(N-P_3)$, comprising:

a transmitter, a receiver, and storage for storing a low-density parity-check (LDPC) mother code definition;

a plurality of memory elements that in combination store a puncture sequence S_3 that corresponds to R_3;

a first set of computer instructions for retrieving a first subset of the plurality of memory elements to yield a puncture sequence S_1 that corresponds to R_1; and

a second set of computer instructions for retrieving a second subset of the plurality of memory elements to yield a puncture sequence S_2 that corresponds to R_2.

12.(Previously Presented) A computer program embodied on a computer readable medium for determining a puncture sequence for a codeword, comprising:

a first storage location for storing a low-density parity-check (LDPC) mother code definition;

a second storage location for storing a plurality of memory elements M_{all} that in combination comprise a maximum rate puncture sequence S_{max} that corresponds to a maximum code rate R_{max}; and

a first set of computer instructions for reading a first subset of memory elements M_{set1}, wherein the number of M_{set1} is less than the number of M_{all}, wherein M_{set1} comprises a puncturing sequence S_1 that corresponds to a code rate $R_1 < R_{max}$.

13.(Original) The computer program of claim 12 further comprising a second set of computer instructions for reading a second subset of memory elements M_{set2}, wherein the number of M_{set2} is greater than the number of M_{set1}, wherein M_{set2} comprises a puncturing sequence S_2 that corresponds to a code rate $R_2 > R_1$, and further wherein at least one memory element is a memory element of both M_{set1} and M_{set2}.

14.(Original) A method for determining a puncture sequence for an ensemble of low-density parity-check (LDPC) codes comprising:

selecting at least one design criteria for an ensemble of LDPC codes and a stop criteria;

calculating a mean input LLR values, m_{u_0}, that achieves the design criteria on the ensemble of codes;

selecting a variable degree j within the design criteria for puncturing that requires one of a smallest mean input LLR value or a smallest decoding complexity;

appending the variable degree to the puncturing sequence;

adjusting the puncturing probability for the punctured variable degree, $\pi_j^{(0)}$; and

repeating the calculating and subsequent steps until the stop criteria is reached.

15.(Original) The method of claim 14 wherein adjusting the puncturing probability for the punctured variable degree, $\pi_j^{(0)}$ includes accounting for a specific code length and a finite number of variable nodes of each variable degree.

16.(Original) The method of claim 14 wherein the stop criteria comprises a code rate equal to one.

17.(Original) The method of claim 14 wherein the stop criteria comprises a length of a puncturing sequence that corresponds to a Binary Erasure Channel (BEC) threshold for random errors.

18.(Original) The method of claim 17 wherein the stop criteria comprises a fraction of punctured variable nodes that reaches or exceeds the BEC threshold.

19.(Original) The method of claim 14 wherein the at least one design criteria is selected from at least one of the group consisting of: a target bit error rate (BER) within a finite number of iterations; an asymptotic E_b/N_0 threshold; and a number of decoding iterations for a target BER.

20.(Currently Amended) A transmitter comprising:

an information source for providing a codeword;

a memory for storing a low density parity check code LDPC mother code definition and a maximum puncture sequence S_{max};

a LDPC encoder having an input coupled to an output of the information source and an input coupled to an output of the memory; and

a modulator having an input coupled to an output of the LDPC encoder,

wherein the encoder operates in one instance to encode at a maximum rate R_{max} by puncturing at least one elements of a codeword ~~in locations~~ described by the maximum puncture sequence S_{max} read from the memory, and in another instance to encode at a lesser

rate R_1 by puncturing elements of a codeword ~~in locations~~ described by a sequence ~~subset~~ S_1 of the maximum puncture sequence S_{max} read from the memory, wherein the maximum puncture sequence S_{max} is stored in and retrieved a plurality of memory elements and the subset S_1 is retrieved from a portion of the plurality of memory elements.

21.(Previously Presented) The transmitter of claim 20, wherein the encoder encodes at any of rates R_{max}, R_3, R_2, and R_1 by puncturing elements of a codeword in locations described by the respective sequences S_{max}, S_3, S_2, and S_1, wherein $R_{max}>R_3>R_2>R_1$ and $S_1 \subseteq S_2 \subseteq S_3 \subseteq S_{max}$.

22.(Currently Amended) The transmitter of claim 20, wherein the encoder encodes at any of rates R_{max}, R_3, R_2, and R_1 by puncturing elements of a codeword in locations described by the respective sequences S_{max}, S_3, S_2, and S_1, wherein $R_{max}>R_3>R_2>R_1$ and each of the sequences S_1, S_2 and S_3 are subsets of S_{max} but not subsets of any of the other of the sequences S_1, S_2 and S_3.

23.(Currently Amended) A receiver comprising:

a demodulator for demodulating a received codeword;

a memory for storing a low density parity check code LDPC mother code definition and a maximum puncture sequence S_{max}; and

a LDPC decoder having an input coupled to an output of the demodulator and an input coupled to an output of the memory;

wherein the decoder operates in one instance to decode at a maximum rate R_{max} by de-puncturing elements of a codeword ~~in locations~~ described by the maximum puncture sequence S_{max} read from the memory, and in another instance to decode at a lesser rate R_1 by de-puncturing at least one element~~s~~ of a codeword ~~in locations~~ described by a sequence ~~subset~~ S_1 of the maximum puncture sequence S_{max} read from the memory, wherein the maximum puncture sequence S_{max} is stored in and retrieved from a plurality of memory elements, wherein the sequence S_1 is retrieved from fewer than all of the memory elements of the plurality of memory elements.

24.(Currently Amended) The receiver of claim 23, wherein the decoder decodes at any of rates R_{max}, R_3, R_2, and R_1 by de-puncturing elements of a codeword in locations described

by the respective sequences S_{max}, S_3, S_2, and S_1, wherein $R_{max}>R_3>R_2>R_1$ and $S_1 \subseteq S_2 \subseteq S_3 \subseteq S_{max}$, wherein the sequences S_2 and S_3 are retrieved from fewer than all of the memory elements of the plurality of memory elements.

25.(Currently Amended) The receiver of claim 23, wherein the decoder decodes at any of rates R_{max}, R_3, R_2, and R_1 by de-puncturing elements of a codeword in locations described by the respective sequences S_{max}, S_3, S_2, and S_1, wherein $R_{max}>R_3>R_2>R_1$ and each of sequences S_1, S_2 and S_3 are subsets of S_{max} but not subsets of any of the other of sequences S_1, S_2 and S_3, wherein the sequences S_2 and S_3 are retrieved from fewer than all of the memory elements of the plurality of memory elements.

26.(Currently Amended) The communication unit of claim 4 wherein each sequence S_i comprises at least one memory element, and there is at least one sequence S_i that has no memory elements in common with another sequence S_i.

27.(Currently Amended) The communication unit of claim 4, wherein the sequence ~~subset~~ S_i corresponds to a puncture sequence representing non-zero element locations in a column of a ~~check~~ parity check matrix.

28. (Currently Amended) The communication unit of claim 4, wherein the sequence ~~subset~~ S_i corresponds to a puncture sequence representing a number of non-zero elements in a column of a ~~check~~ parity check matrix.

29. (Currently Amended) The communication unit of claim 4, wherein different combinations of columns of a check parity matrix correspond to different sequences ~~subsets~~ S_i and all columns of the ~~check~~ parity check matrix correspond to the maximum puncture sequence S_{max}.

30.(Currently Amended) A method for operating a communication unit at multiple code rates comprising:

receiving a codeword defining N codeword elements and K information elements coded at a code rate R=K/(N-P), wherein P is a number of punctured elements of the codeword;

retrieving an error reduction code mother code definition from a first storage location;

retrieving a puncture sequence from a second storage location, wherein the puncture sequence retrieved from the second storage location is a selected one of a maximum puncture sequence S_{max} for a maximum code rate S_{max} and a minimum puncture sequence S_1 for a minimum code rate R_1 and the minimum puncture sequence S_1 is a subset of S_{max} and the minimum puncture sequence S_1 corresponds to a column of a ~~check~~ parity check matrix, wherein the maximum puncture sequence is stored in and retrieved from a combination of memory elements and the minimum puncture sequence S_1 is stored in and retrieved from a subset of the combination of memory elements.

31. (New) A circuit, comprising:

a plurality of memory elements adapted to store a puncture sequence S_{max}, the puncture sequence S_{max} corresponding to a maximum code rate R_{max}, the puncture sequence S_{max} being stored in a memory, a puncture sequence S_1 being retrieved from a subset of the plurality of memory elements adapted to store the puncture sequence S_{max}, the puncture sequence S_1 corresponding to a code rate R_1 that is less than the maximum code rate R_{max}; and

circuitry adapted to perform one of encoding and decoding a codeword defining N codeword elements and K information elements coded at a code rate R=K/(N-P), where P is a number of punctured elements of the codeword and the code rate R includes the code rates R_{max} and R_1.

32. (New) A circuit according to claim 31, further comprising a puncture sequence S_2 being retrieved from another subset of the plurality of memory elements, the puncture sequence S_2 corresponding to a code rate R_2 that is less than the maximum code rate R_{max}.

33. (New) A circuit according to claim 31, wherein the subset of the plurality of memory elements adapted to store the puncture sequence S_1 are contiguous memory elements.

34. (New) A circuit according to claim 32, wherein the subset of the plurality of memory elements adapted to store the puncture sequence S_2 has no memory elements in common with the subset of the plurality of memory elements adapted to store the puncture sequence S_1.

35. (New) A circuit according to claim 32, wherein the code rate R_2 is different from code rate R_1.

36. (New) A circuit according to claim 32, wherein the code rate R_2 is greater than code rate R_1.

37. (New) A circuit according to claim 31, wherein the circuitry in one instance decodes the codeword at a maximum rate R_{max} by de-puncturing at least one codeword element according to the maximum puncture sequence S_{max} read from the plurality of memory elements, and in another instance decodes the codeword at a lesser rate R_1 by de-puncturing at least one codeword element according to the sequence S_1 read from the subset of the plurality of memory elements.

38. (New) A circuit according to claim 31, wherein the circuitry operates in one instance encodes the codeword at a maximum rate R_{max} by puncturing at least one codeword element according to the maximum puncture sequence S_{max} read from the plurality of memory elements, and in another instance encodes the codeword at a lesser rate R_1 by puncturing at least one codeword element according to the sequence S_1 read from the subset of the plurality of memory elements.